APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/394,011	09/10/1999	HERMAN LEE BLACKMON	RO999-080	3617

7590 06/22/2004	EXAMINER
KARUNA OJANEN IBM CORPORATION DEPT 917 3605 HIGHWAY 52 NORTH ROCHESTER, MN 559017829	VITAL, PIERRE M

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 06/22/2004

17

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
	09/394,011	BLACKMON ET AL.
Office Action Summary	Examiner	Art Unit
	Pierre M. Vital	2188

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17,19 and 20* is/are allowed.

6)☒ Claim(s) *1-16,18 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Response to Amendment

1.   This Office Action is in response to applicant's communication filed May 10, 2004 in response to PTO Office Action mailed February 6, 2004. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2.   Claims 1-21 have been presented for examination in this application. In response to the last Office Action, claims 19 and 21 have been amended. No claims have been canceled or added. As a result, claims 1-21 are now pending in this application.

Response to Arguments

3.   Applicant's arguments, see Paper No. 16, filed May 10, 2004, with respect to the rejection(s) of claim(s) 1-21 under the Howe reference have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Au (5,729,718).

Claim Objections

4.   Claim 21 is objected to because of the following informalities:

In line 17, before "determine", please insert –to--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

6.   Claims 1-16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Stracovsky et al (US6,385,708) and Harriman et al (US6,088,772) and Au

(5,729,718).

As per claim 1, Stracovsky discloses a method for processing commands in a

computer memory subsystem comprising (a) receiving a plurality of commands on a bus

network connected to said memory subsystem [*processors 102 generate memory address*

requests; col. 6, lines 1-19]; (b) categorizing said received commands into command

types [*interface 110 converts received command and address a universal command 200 which contains*

5 data fields: pre-charge, activate, read, write, refresh; col. 6, lines 30-43; col. 8, lines 22-24];

(d) determining memory cycle performance penalties of said categorized commands in

each of said queues [*earliest issue time and data occurrence time associated with the commands are*

determined; col. 3, lines 2-11]; (f) determining if each of said selected command is valid

[*data occurrence time and durations of the command ready to be issued are compared with data*

occurrence time and durations previously issued commands to detect collisions; col. 20, lines 11-28];

(g) arbitrating said valid commands and selecting one of said valid commands to

execute [*when a command is issued, addresses for lower priority commands are shifted into higher*

priority positions; command with highest priority based on the comparison is issued; col. 20, lines 34-

50].

However, Stracovsky does not specifically teach (c) placing each received

command into a queue pertaining to its respective command type; (e) reordering said

categorized commands in each of said queues so that one categorized command in

each of said queues having the least memory cycle performance penalty is selected for

execution; and (h) executing sequential valid commands of the same command type as

recited in the claim.

Harriman discloses (c) placing each received command into a queue pertaining

to its respective command type [*command queue block has three separate command queues, a*

normal priority read queue 316, a normal priority write queue 318, and a high priority read or write queue

318; col. 4, lines 31-67]; (h) executing sequential valid commands of the same

command type [*high priority data is returned in order;* col. 3, lines 21-25, col. 5, lines 65-66] to

provide an adequate command reordering mechanism which balances latency and

bandwidth concerns while optimizing based on performance criteria such as locality of

reference and/or command type (col. 2, lines 28-31). Thus, it would have been obvious

to one of ordinary skill in the art, having the teachings of Stracovsky and Harriman

before him at the time the invention was made, to modify the system of Stracovsky to

include placing each received command into a queue pertaining to its respective

command type and executing sequential valid commands of the same command type

because it was well known to provide an adequate command reordering mechanism

which balances latency and bandwidth concerns while optimizing based on

performance criteria such as locality of reference and/or command type as taught by Harriman.

However, the combination of Stracovsky and Harriman does not specifically teach reordering categorized commands in each of said queues so that one categorized command in each of said queues having the least memory cycle performance penalty is selected for execution as recited in the claim.

Au discloses reordering commands in a queue so that one command having the least memory cycle performance penalty is selected for execution to increase I/O throughput by minimizing latency between transfers (*the command having the least time latency is selected and promoted to the front of the queue*; col. 1, lines 60 – col. 2, line 13; col. 4, lines 1-5).

Since the technology for implementing the reordering of commands in a queue so that the command having the least memory cycle penalty is selected for execution was well known, and since the reordering of commands in a queue so that the command having the least memory cycle penalty is selected for execution increase I/O throughput by minimizing latency between transfers, an artisan would have been motivated to use the Au's reordering technique in the system of Stracovsky and Harriman. Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of Stracovsky and Harriman and Au before him at the time the invention was made, to modify the system of Stracovsky and Harriman to include the reordering of commands in a queue so that the command having the least memory cycle penalty is

selected for execution because it was well know to increase I/O throughput by

minimizing latency between transfers as taught by Au.

As per claim 2, Stracovsky discloses said command types are forms of store and

fetch commands [col. 12, line 58].

As per claim 3, Stracovsky discloses said command types are associated with a

particular source or destination of said received memory commands [col. 7, lines 61-

col. 8, line 26].

As per claim 4, Stracovsky discloses said particular source or destination is a

particular computer processor connected on said bus [col. 6, lines 7-10].

As per claim 5, the concept of a particular source or destination being an I/O hub

controller functionally connected on a bus is well known in the state of the art.

As per claim 6, the concept of a particular source or destination being a switching

fabric connected to a bus is well known in the state of the art.

As per claim 7, the concept of a particular source or destination being a

compression/decompression engine functionally connected to a bus is well known in the

state of the art.

As per claim 8, Stracovsky discloses said command types, which originate from

or are required for a particular application, have priority [col. 8, lines 30-33].

As per claim 9, Stracovsky discloses said step of receiving a plurality of

commands further comprises determining if any of said received commands have an

address dependency and passing said address dependency determination with said

memory command [col. 6, lines 13-20].

As per claim 10, Stracovsky discloses said step of determining memory cycle

performance penalties of said categorized commands further comprises comparing a

number of oldest received categorized commands with each other [col. 20. lines 45-50].

As per claim 11, Stracovsky discloses said step of determining memory cycle

performance penalties of said categorized commands further comprises comparing a

number of oldest received categorized commands with a currently chosen command

[col. 18, lines 1-7].

As per claim 12, Stracovsky discloses said step of determining memory cycle

performance penalties of said categorized commands further comprises comparing a

number of oldest received categorized commands with a previously chosen command

[col. 20, lines 13-28].

As per claim 13, Stracovsky discloses said step of reordering said categorized

commands further comprises selecting the oldest of said categorized commands that

have the least memory cycle performance penalty for execution [col. 20, lines 45-50].

As per claim 14, Harriman discloses said step of arbitrating said reordered valid

commands further comprises granting priority to said type of command having said least

memory cycle performance penalty [col. 4, lines 2-5].

As per claim 15, Harriman discloses said step of arbitrating said reordered valid

commands further comprises granting priority to a command type other than said

command type of said reordered valid commands [col. 7, lines 20-24].

As per claim 16, Harriman discloses said step of executing sequential valid commands of the same command type further continues until a valid memory command of said command type is no longer available, or until a predetermined number has been executed, or until a memory command of another of said command types has higher priority [col. 3, lines 44-64].

Claim 18 is rejected as per claims 1 and 16 above.

7.   Claim 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stracovsky et al (US6,385,708) and Harriman et al (US6,088,772).

As per claim 21, discloses a computer memory controller, comprising:

(a) means to receive a plurality of types of memory commands from a plurality of command sources [*processors 102 generate memory address requests*; col. 6, lines 1-19];

(b) means to determine the memory cycle performance penalty associated with each memory command of each of said plurality of types [*earliest issue time and data occurrence time associated with the commands are determined*; col. 3, lines 2-11];

(c) means to compare said memory commands of each of said types with other memory commands of the same type to determine which of said memory commands have the least memory cycle performance penalty [*group selector determines to which group a particular request belongs*; col. 8, lines 22-24; col. 20, lines 45-50];

(d) means to compare said memory commands of each of said types with a current chosen memory command of the same type to determine which of said memory commands have the least memory cycle performance penalty [*commands 1, 2, 3, are compared and reordered 1, 3, 2*; col. 18, lines 1-7];

(e) means to compare said memory commands of each of said types with a previously chosen memory command of the same type to determine which of said memory commands have the least memory cycle performance penalty [*data occurrence time and duration are compared with five previously issued commands*; col. 20, lines 13-28];

(f) means to select one of said memory commands having the least memory cycle performance penalty by selecting the oldest [*the oldest one is issued*; col. 20, lines 47-50].

However, Stracovsky does not specifically teach means to continue execution of memory commands of the same type as said selected memory command as recited in the claim.

Harriman discloses executing sequential valid commands of the same command type to provide high bandwidth improvements with a resulting increase in latencies (col. 3, lines 21-25, col. 5, lines 65-66). Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of Stracovsky and Harriman before him at the time the invention was made, to modify the system of Stracovsky to include executing sequential valid commands of the same command type because it was well known to provide high bandwidth improvements with a resulting increase in latencies as taught by Harriman.

Allowable Subject Matter

8.   Claims 17 and 19-20 are allowed.

9.   The following is a statement of reasons for the indication of allowable subject

matter:

As per claims 17 and 19, the prior art of record does not teach or suggest

"determining memory cycle performance penalties of categorized commands by

comparing a number of oldest received categorized commands with each other, with a

currently chosen command, and with a previously chosen command" in combination

with the other elements set forth in the claimed invention.

Therefore, dependent claim 20 is allowable as being dependent upon

independent claim 19 and having additional allowable features therein.

Conclusion

10.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111 (c) to consider

these references fully when responding to this action. The documents cited therein

teach command reordering and granting priority to commands having least memory
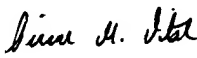
cycle performance penalty.

11.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 17, 2004

Pierre M. Vital
Examiner
Art Unit 2188